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EFFICIENT IMPLEMENTATION OF 18T COMPRESSOR FOR MULTIPLIER APPLICATIONS

S. Vasu Krishna[1] and K. Lal Kishore[2]

Abstract - This paper presents the design of compressor which is able to operate at ultra-low voltage. In this method XOR-XNOR gates with MUX design can be modified with CMOS transistors. The proposed method utilizes the adder circuit with minimum number of transistors, mostly used in digital circuits and high speed applications. The proposed method introduces an effective area and power efficient adder with minimum usage of transistor circuit in place of traditional adder. This full adder is implemented in different kind of multipliers such as Array multiplier, Wallace Tree multiplier and Baugh Wooley multiplier. Existing and proposed circuits are simulated using Cadence 180nm technology at supply voltage of 1.8v and 5MHz frequency. With the help of proposed adder circuit, area and power can be minimized in the multiplier architectures. The results obtained are compared with the existing methods.
Keywords: XOR-XNOR, MUX and CMOS

I. INTRODUCTION

Now-a-days, there is an enormous increase of mobile electronic gadgets ready for multimedia environments such as laptops, portable cellular system and tablets. Similarly, Personal Communication Services (PCS) are also demanding such as pocket size devices, sophisticated modems and digital networks [1]. In VLSI systems, fast arithmetic computation cells like multipliers and adders are used extensively. To attain the filtering and convolution algorithm, we wanted floating point units and generic logic units [2]. There is a need to design multiplier circuit for high speed application [3]. Basically, the analog circuits are converted to digital circuits in wireless communication circuitry to avoid power loss. In digital signal processing, we need to explore high speed and low power communication in the sub-micron CMOS technology [4].

In the conventional mode of operation totally 28 transistors can be used in CMOS technology. Self Energy Recovery Full adder (SERF), which consists of 10 transistors, that is few number of transistors is introduced. This adder has a threshold loss problem compared to the complementary static CMOS adders. For example, VDD logic value is not 1 and similarly the ground value may not be zero. This kind of threshold loss of the CMOS transistor will affect the CMOS logic circuits [5].The compressor is one unit, which minimizes the latency problem in CMOS circuits. Without usage of proper adder circuits, we cannot expect power and speed to be in optimum range [6]. In this investigation, the main concentration is on the Full Adder (FA) logic cells, which are used in arithmetic circuits. CMOS is looked upon as the preferred choice for low power applications [7].

Power, area and delay are major parameters to design any type of VLSI logic circuits. With use of the process, technology scaling is not possible to minimize these parameters. So an optimization technique to improve the speed and performance of the logic circuits is needed. This will minimize the range of power and area usage [8]. The XOR (4T) based hybrid-CMOS FA has been introduced to provide better performance compared to the

[1] *Department of Electronics and Communication Engineering, Geethanjali College of Engineering and Technology, Hyderabad, Telangana, India*
[2] *Department of Electronics and Communication Engineering, CVR College of Engineering, Hyderabad, Telangana, India*

other FA cells. Here different adder logic circuits were implemented, simulated, analyzed and compared [9]. High Speed, Low Power concept is presented for 3-2,4-2 and 5-2 compressors. [10].

A comparative study can be done on different type of logics of the FA circuit, by considering the power, delay, power delay product (PDP) of different FA designs using CMOS Logic Styles. XOR-XNOR type FA scheme will be better than complementary CMOS type and pass transistor design [11]. For some applications, we have to reduce the power consumption, area and delay. To conquer this, our proposed method will be a good solution for reducing the number of transistors and maintain the logic levels required for a Full adder circuit in any type of digital circuit.

II. RELATED WORK

Najafi *et al*. [12] have introduced novel 5:2 compressor architecture for improving the power, delay and area. The proposed architecture contains more number of transistors. Using this architecture, operation speed is high, power consumption is low and latency is reduced. Here, it is not possible to reduce the area since 28 transistors were used.

Radha Shende *et al*. [13] have presented a binary to residue converter based on the 2^k-1 modulo set. This proposed architecture presents a unique feature like easy to perform arithmetic operations. It also improves the speed and decreases the area. This converter uses less hardware and it is simple and fast but more power is consumed.

Mehdi Ghasemzadeh *et al*. [14] have introduced a high speed 5-2 compressor based on new architecture. The main purpose of this paper is to reduce the latency from input to output, and thereby increase the speed of the compressor. Even operation speed is also high but power reduction possibilities are less.

Fazel Sharifi *et al.* [15] have presented a design of quaternary logic 4-2 and 5-2 compressor. The proposed compressor consists of three modules for performing quaternary logic. The new compressor decreases the addition operations delay, reduce the area and complexity of the circuit but power consumption is average.

Sanjeev Kumar *et al.* [16] has presented an improved design of 3-2 compressor for high speed multipliers with reduced power consumption. With the help of proposed compressor, delay and PDP is reduced which leads to better performance of the system. But the circuit is not simple.

III. PROPOSED METHODOLOGY

Compressor is one, which helps in the compression of the data in order to reduce the bandwidth required to any channel for communication system. The main aim of the proposed method is to provide the solution for real time applications by optimizing the power, delay, area. Multiplier is an important fundamental unit in Digital Signal Processing operations such as addition, multiplication, convolution, filtering...etc. Multiplication operation is the basic arithmetic operation in the digital signal processing applications. Some of the researchers have introduced few types of compressors such as 3-2, 4-2 and 5-2 compressors, which require more number of transistors to implement any applications. So our aim is to reduce the number of transistors in the design of compressor unit, this will in turn minimize the area, power and delay of the circuit.

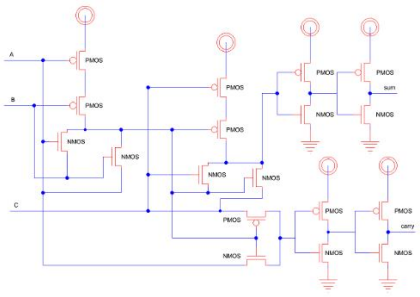

Fig.1. Proposed 18T Full adder Circuit

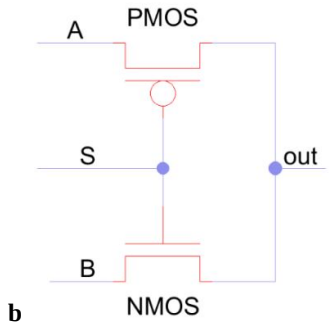

Fig.2. Proposed MUX Circuit

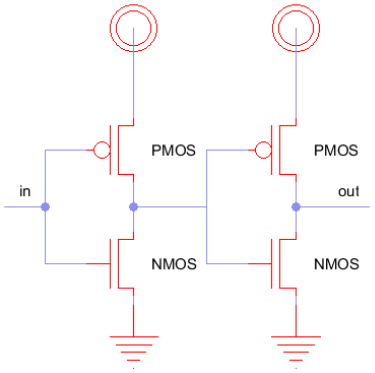

Fig.3. Proposed Threshold Circuit

The schematic diagram of the 3-2 compressor with minimum number of transistors is shown in the Fig.1. To implement full adder circuit, we need two XNOR implementation, one MUX which is given in Fig.2 and threshold circuit which is given in Fig.3. Totally our proposed full adder circuit will require only 18 transistors as we can observe in the Fig.1. Compared to the existing implementations, the number of transistor will be reduced. It also reduces the area, power and delay required for full adder implementation in CMOS technology. Inputs to full adder are A, B and C_{in} and outputs are Sum and C_{out}. We will discuss three different types of multipliers for efficient area, power and with less delay implementations for various applications. We are replacing the full adder in these multipliers, so that it consumes less power, area and delay. Finally proposed method parameters are compared with the existing implementation of the adder circuit.

III.I. MULTIPLIERS

A binary multiplier is one which can be implemented by electronic components such as transistor circuits used in digital electronics in order to multiply two binary numbers. Array multiplier is one which multiplies the array of bits, based on add and shift algorithm. Each stage partial result is originated by the multiplication of the multiplicand with one multiplier bit. After the first bit multiplication, the partial results are shifted according to their bit orders and then added. The schematic diagram of the 4 bit array multiplier is shown in the Fig.4, built of AND gates and four bit adder logic circuits. The operations go on until the MSB bit has reached. The inputs to the array multiplier are $A_0A_1A_2A_3$ and $B_0B_1B_2B_3$ and output of the array multiplier is $Y_0Y_1Y_2Y_3Y_4Y_5Y_6Y_7$.

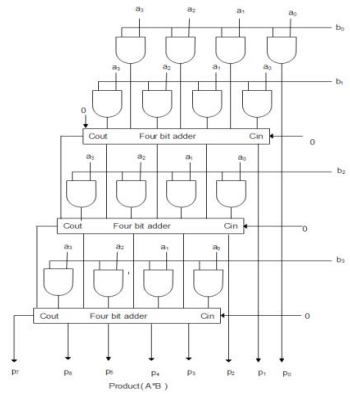

Fig.4. Schematic of 4 bit Array Multiplier

Another type of the multiplier is the Baugh Wooley multiplier and its schematic diagram is shown in the Fig.5. In this 2's complement number multiplication can be done in order to increase the speed of the operation and to minimize the area required for its implementation. Fig.5 is the parallel multiplier, which takes the parallel inputs and gives the parallel outputs, but it consumes significant hardware than serial multiplier. For example $A_1A_2A_3A_4$ and $B_0B_1B_2B_3$ are the two sets of the inputs and $C_0C_1C_2C_3C_4C_5C_6C_7$ are the outputs as we can observe in the Fig.5.

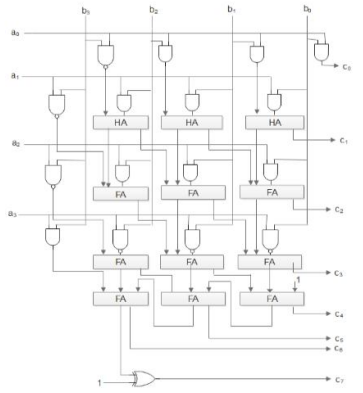

Fig.5. Baugh Wooley Multiplier

A Wallace Tree Multiplier is based on tree structure which minimizes the number of additions in the critical path to O (log n) than O (n). This will minimize the number of adders in Wallace tree multiplier implementation and therefore speed of the operation also increases, so it is an efficient hardware implementation. The Fig.6 shows the schematic implementation of the Wallace tree multiplier. The final product is obtained by several levels of the tree structures. The main aim of using Wallace tree multiplier is to minimize the delay and power of the multiplier circuit.

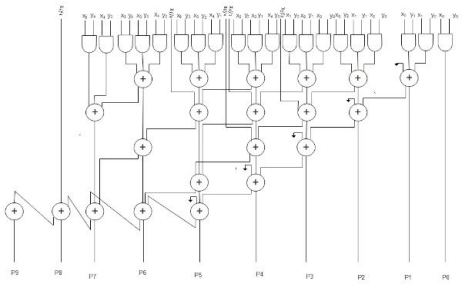

Fig.6. Schematic of Wallace Tree Multiplier

IV. EXPERIMENTAL SETUP

The proposed method uses minimum number of transistors to design an efficient full adder circuit with less area. The circuit design is implemented on Cadence 180nm technology at 1.8V supply voltage and 5MHz frequency. From this Area, Power can be minimized effectively.

V. RESULTS AND DISCUSSION

Table (1), (2) and (3) shows the comparison of
different type of existing multipliers with proposed multiplier, with respect to Area, Power and Delay.
Table 4 denotes the full adder circuit performance of different methods for area, power, delay and number of transistor. As we can observe in the tables power and area required for the proposed method is reduced and speed of the operation is much improved as compared to existing methods.

Table.1. Comparison of Wallace Tree Multiplier with Proposed Method

Wallace Tree multiplier								
Existing [10]			Existing I [12]			Proposed		
Area (um^2)	Power (uW)	Delay (ns)	Area (um^2)	Power (uW)	Delay (ns)	Area (um^2)	Power (uW)	Delay (ns)
190.02	175.38	0.65668	155.46	140.4	0.44717	136.9	74.77	0.58897

Table.2. Comparison of Array Multiplier with Proposed Method

Array multiplier								
Existing[10]			Existing I [12]			Proposed		
Area (um^2)	Power (uW)	Delay (ns)	Area (um^2)	Power (uW)	Delay (ps)	Area (um^2)	Power (uW)	Delay (ns)
190.08	139.68	0.79241	155.54	115.3	1.22388	105.12	92.56	19.6562

Table.3. Comparison of Baugh Wooley Multiplier with Proposed Method

Baugh Wooley multiplier								
Existing[10]			Existing I [12]			Proposed		
Area (um^2)	Power (uW)	Delay (ns)	Area (um^2)	Power (uW)	Delay (ps)	Area (um^2)	Power (uW)	Delay (ns)
170.64	131.36	0.6441	140.7	108.7	0.875389	102.96	94.39	0.92412

Table.4. Comparison for Area, Power, Delay and NT for different methods

Specification	Existing [10]	Existing- I [12]	Proposed
Area (um^2)	12.96	10.08	6.48
Power (nw)	$11.64*10\text{-}^{6}$	10.5810-^{6}	$8.54*10\text{-}^{6}$
Delay (ns)	0.132612	0.252391	0.213284
Number of transistor (NT)	36	28	18

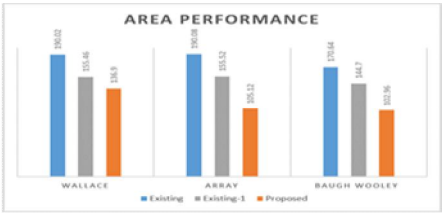

Fig.7. Area Performance for different Multipliers

Fig.8. Power Performance for different Multipliers

Area and power performance of the three multipliers is shown in Fig.7 and Fig.8. It clearly shows that area and power is reduced in the proposed method compared to existing methods.

VI. CONCLUSION

The architecture of the different kinds of multipliers is analysed using CMOS implementation of XOR-XNOR, MUX and threshold circuit blocks. The new proposed full adder circuit has been implemented in the different multipliers discussed. With the help of new full adder circuit, the area and power is minimized in the multiplier circuit.

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